4

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/689,265 | 10/20/2003 | Brian L. Smith | 5681-11500 | 2888 |

35690 7590 02/01/2007

MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL, P.C.
700 LAVACA, SUITE 800
AUSTIN, TX 78701

| EXAMINER | |
|---|---|
| RADOSEVICH, STEVEN D | |
| **ART UNIT** | **PAPER NUMBER** |
| 2138 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 02/01/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/689,265 | SMITH, BRIAN L. | |
| | Examiner | Art Unit | |
| | Steven D. Radosevich | 2138 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *17 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19 and 20* is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

Claims 1-20 are present for examination within this instant office action, which is in response to applicant's correspondence with the U.S.P.T.O. on 10/19/06 in response to the office action mailed to the applicant on 7/17/2006.

### *Response to Arguments*

Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Theodoras II et al (U.S. Patent 6684350 B1) filed on 12/22/2000.

1. As per claims 1, 7, and 13, Theodoras teaches.

Storing a first value (first pattern block 810 in figure 8 and column 11 lines 20-26 with column 7 lines 31-35);

Storing a second value (second pattern block 820 in figure 8 and column 11 lines 20-26 with column 7 lines 31-35);

Receiving a clock signal (timing in column 11 lines 25-26 along with table 2 in column 10);

Selecting either said first value or said second value for inclusion in a test pattern in response to said clock signal (figure 8, column 11 lines 20-26, and table 2 in column 10);

Wherein determining whether to select either said first value or said second value on a given clock cycle is determined according to a predetermined test pattern sequence (column 11 line 35 and lines 21-23, column 10 lines 24-53 including table 2, and column 3 lines 59-61).

2. As per claims 2 and 14, Theodoras teaches wherein said test pattern sequence comprises a plurality of indication, each of said indication indicating either said first value or said second value (column 11 lines 20-26 along with figure 8).

3. As per claim 3, Theodoras teaches wherein said first value is stored in a first register location, and said second value is stored in a second register location, and wherein both said first and second register locations correspond to a same link signal line (figure 8 and column 11 lines 20-27).

4. As per claim 4, Theodoras teaches further comprising driving value of said test pattern from a first component to a second component (figure 8, column 11 lines 20-27).

5. As per claims 5, 8-12, and 15-17, Theodoras teaches wherein each of said first component and second component alternate driving values of said test pattern during a sixteen test cycle sequence (column 11 lines 5-12).

6. As per claim 6, Theodoras teaches wherein said alternate driving values by said first component and said second component is separated by one or more turn around cycles (table 2 in column 10 an column 11 lines 20-27).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Theodoras II et al (U.S. Patent 6684350) as applied to claim 13 above, and as evidenced by Fontenot et al (U.S. Patent 6076177) or Tomari (U.S. Patent 6480979 B1).

7. As per claim 18, Theodoras teaches the component as recited above with respect to claim 13 comprising drivers, register, test pattern sequence unit, and control circuitry.

Theodoras does not specifically teach wherein the component further comprises a plurality of receivers coupled to said link, and wherein said component includes pattern checking circuitry configured to compare values received via said link to expected values.

However those of ordinary skill within the art at the time the invention was made would recognize a plurality of receivers coupled to said link and said component including pattern checking circuitry configured to compare values

received via said link to expected values is well known. The art is replete with references that teach parallel testing by a single tester to reduce testing time along with built-in system testing (BIST) and/or evaluation of test results from DUT (devices unit test) by a tester, see for example Tomari and/or Fontenot.

Therefore those of ordinary skill within the art at the time the invention was made would have been motivated to comprise a plurality of receivers coupled to Theodoras' link to implement parallel testing that reduces testing time of multiple components being tested. Additionally, those of ordinary skill within the art at the time the invention was made would have been motivated to include pattern checking circuitry configured to compare values received via said link to expected values within Theodoras' component (tester) to evaluate and determine the functionality of the multiple components being tested, which those in the art would recognize is the point behind circuit testing.

***Allowable Subject Matter***

Claims 19 and 20 are allowed.

The present invention at this point pertains to a component comprising a test pattern generator using a single register holding two different first and second bit patterns.

The claimed invention recites features such as: 1) the register comprising N bits, wherein said first and second bit patterns comprises N/2 or half the register bits, and wherein each signal line corresponds to one bit from each of the first and second bit patterns. 2) The signal line is coupled to receive a value from a multiplexer, which is controlled via the control circuit to select which bit at

a given time is selected between either the first or second bit patterns within the register.

The prior art of record teaches test pattern generation wherein different test patterns are used and selected between in the generation of the test pattern. However the prior art fails to teach the register comprising N bits wherein a first and second bit patterns comprise N/2 or half the register bits, and wherein each of a number of signal lines corresponds to only a single bit from each of the first and second bit patterns. Hence, the prior art of record fails to anticipate or render obvious the claimed invention. Thus claims 19 and 20 are allowable over the prior art of record.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven D. Radosevich whose telephone number is 571-272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven D. Radosevich
Examiner
Art Unit 2138

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100